Listing and Amendments to the Specification

Please amend the paragraph at p. 3, line 30 to p. 4, line 11 in the Specification to read as follows:

FIG. 2 is a block diagram of an exemplary wireless receiver. An incoming modulated or encoded analog signal received at an antenna 25 is received into the reception circuitry board 23 containing a frequency synthesizer for synchronizing the receiver to an exemplary transmitter carrier frequency in the range of 900 MHz. The encoded signal is decoded by an eight-to-fourteen modulation decoder 22. Eight-to-fourteen EFM encoding is a known encoding technique for compact disk CD encoding. A digital audio stream I2S from the decoder 22 is changed by the stereo digital-to-analog converter DAC 21 into an analog stereo input signal to an audio system. Communications protocols between the decoder 22 and processor 24 preferably conform to known I2C bus protocols. The processor is preferably a microprocessor tied over a microwire bus to the reception circuitry 23. The processor controls the frequency synthesizer for synchronizing the receiver to the radio carrier frequency of the audio file signal source transmitter. The microprocessor continually queries the EFM decoder and determines whether the decoder's EFM PLL is locked or unlocked. If the EFM PLL is unlocked, then the microprocessor will perform an EFM decoder soft reset and re-initialization. The processor 24 ~~also~~ carries out the inventive wireless audio file signal loss detection and resetting and initialization of the decoder 22 when a loss of the wireless audio file signal is detected.